What is claimed is:

1. A method of forming a select line in a NAND type flash memory device, comprising the steps of:

sequentially forming a tunnel oxide film and a first polysilicon layer on a semiconductor substrate in which an isolation film is formed, and then performing a first patterning process in the direction of bit lines;

forming a dielectric film, a second polysilicon layer and a silicide layer on the entire structure;

performing a second patterning process for the silicide layer and the second polysilicon layer so that a first projection is formed at the edge of the silicide layer and the second polysilicon layer on the device isolation region between drain select line regions;

performing a third patterning process for the dielectric film and the first polysilicon layer to form drain select lines so that a second projection the one end of which overlaps the first projection is formed at the edge of the first polysilicon layer on the device isolation region between the drain select lines regions;

forming an interlayer insulating film on the entire structure and then forming a contact hole through which the first and second projections are opened; and

burying the contact hole with a conductive material to form contact plugs and also forming a metal line connecting the contact plugs formed on the first and second projections on the interlayer insulating film.

2. The method as claimed in claim 1, wherein during the second patterning process, in the cell region, the silicide layer and the second polysilicon layer are patterned in order to form word lines.

3. The method as claimed in claim 1, wherein the third patterning process is performed with the etch mask formed on the second projection so that the second projection is formed at the edge of the first polysilicon layer.

4. The method as claimed in claim 1, wherein during the third patterning process, in the cell region, a self-aligned etch process is performed in order to form the word lines, whereby the dielectric film and the first polysilicon layer are patterned.

5. The method as claimed in claim 1, further comprising the step of forming insulating film spacers at the sidewalls of the drain select lines, before the interlayer insulating film is formed after the third patterning process.

6. The method as claimed in claim 1, wherein upon formation of the contact hole and the contact plug, the contact hole and the contact plugs for connecting the bit line and the active region are formed even at the active region of the cell region.

7. A method of forming a select line in a NAND type flash memory device, comprising the steps of:

sequentially forming a tunnel oxide film and a first polysilicon layer on a semiconductor substrate in which an isolation film is formed, and then performing a first patterning process in the direction of bit lines;

forming a dielectric film, a second polysilicon layer and a silicide layer on the entire structure;

performing a second patterning process for the silicide layer and the second polysilicon layer by means of an etch process using a control gate mask;

forming an interlayer insulating film on the entire structure and then forming a contact hole through which a given portion of the first and second polysilicon layer is opened; and

burying the contact hole with a conductive material to form contact plugs and also forming a metal line connecting the contact plugs formed on the first and second projections on the interlayer insulating film.

8. The method as claimed in claim 7, wherein during the second patterning process, in the cell region, the silicide layer and the second polysilicon layer are patterned in order to form word lines.

9. The method as claimed in claim 7, further comprising the step of performing a third patterning process for the dielectric film and the first polysilicon layer in the cell region by means of the self-aligned etch process, before the interlayer insulating film is formed after the second patterning process.

10. The method as claimed in claim 7, further comprising the step of forming insulating film spacers at the sidewalls of the source select line, before the interlayer insulating film is formed after the second patterning process.

11. The method as claimed in claim 7, wherein upon formation of the contact hole and the contact plug, the contact hole and the contact plugs for connecting the bit line and the active region are formed even at the active region of the cell region.